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Shinya SASAGAWA et al.	)
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For: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE	) Not Yet Assigned

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Yui Minato, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the US Patent Application No. 10/731,089 filed on December 10, 2003; and

that to the best of my knowledge and belief the followings is a true and correct translation of the US Patent Application No. 10/731,089 filed on December 10, 2003.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 15th day of June 2004

Yui Minato

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[Name of Document] Specification

[Title of the Invention] METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

[Scope of Claim]

[Claim 1]

A method of manufacturing a semiconductor device, comprising:

a process of forming a mask pattern on a laminate comprising a lower first conductive layer and an upper second conductive layer;

a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of the laminate;

a plasma treatment to be performed to the first conductive layer pattern; and

a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form a second conductive layer pattern.

[Claim 2]

The method according to claim 1, wherein the plasma treatment is an argon plasma treatment.

[Claim 3]

The method according to claim 1, wherein a reaction product adhering to a sidewall portion of the first conductive layer pattern is removed by the plasma treatment.

[Claim 4]

The method according to claim 1, wherein the first conductive layer is metal nitride.

[Claim 5]

A method of manufacturing a semiconductor device, comprising:

a process of forming a mask pattern on a laminate comprising a lower first conductive layer and an upper second conductive layer including titanium or including titanium as its main component;

a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of the laminate;

a plasma treatment to be performed to the first conductive layer pattern; and

a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form a second conductive layer pattern.

[Claim 6]

The method according to claim 5, wherein the plasma treatment is an argon plasma treatment.

[Claim 7]

The method according to claim 5, wherein a reaction product adhering to a sidewall portion of the first conductive layer pattern is removed by the plasma treatment.

[Claim 8]

The method according to claim 5, wherein the first conductive layer is metal nitride.

[Claim 9]

A method of manufacturing a semiconductor device, comprising:

a process of forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer on the first conductive layer, and a third conductive layer on the second conductive layer;

a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of the laminate;

a plasma treatment to be performed to the first conductive layer pattern; and

a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form a second conductive layer pattern.

[Claim 10]

The method according to claim 5, wherein the plasma treatment is an argon plasma treatment.

[Claim 11]

The method according to claim 5, wherein a reaction product adhering to a sidewall portion of the first conductive layer pattern is removed by the plasma treatment.

[Claim 12]

The method according to claim 5, wherein the first conductive layer is metal nitride.

[Claim 13]

The method according to claim 5, wherein the third conductive layer is a metal having high-melting point.

[Claim 14]

A method of manufacturing a semiconductor device, comprising:

a process of forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer including titanium or including titanium as its main component on the first conductive layer, and a third conductive layer on the second conductive layer;

a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of the laminate;

a plasma treatment to be performed to the first conductive layer pattern; and

a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form a second conductive layer pattern.

[Claim 15]

The method according to claim 14, wherein the plasma treatment is an argon plasma treatment.

[Claim 16]

The method according to claim 14, wherein a reaction product adhering to a sidewall portion of the first conductive layer pattern is removed by the plasma treatment.

[Claim 17]

The method according to claim 14, wherein the first conductive layer is metal nitride.

[Claim 18]

The method according to claim 14, wherein the third conductive layer is a metal having high-melting point.

[Claim 19]

A method of manufacturing a semiconductor device, comprising:

a process of forming a mask pattern on a laminate comprising a lower first conductive layer and an upper second conductive layer over a semiconductor layer with a

gate insulating film interposed therebetween;

a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of the laminate;

a plasma treatment to be performed to the first conductive layer pattern;

a second etching process for subjecting the first conductive layer pattern to anisotropic etching to form a second conductive layer pattern; and

a process of adding an impurity to the semiconductor layer with the second conductive layer in the second conductive layer pattern as a shielding mask to form a region to which the impurity is added in the semiconductor film, which overlaps with the first conductive layer in the second conductive layer pattern.

[Claim 20]

The method according to claim 19, wherein the plasma treatment is an argon plasma treatment.

[Claim 21]

The method according to claim 19, wherein a reaction product adhering to a sidewall portion of the first conductive layer pattern is removed by the plasma treatment.

[Claim 22]

The method according to claim 19, wherein the first conductive layer is metal nitride.

[Claim 23]

A method of manufacturing a semiconductor device, comprising:

a process of forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer on the first conductive layer, and a third conductive layer on the second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween;

a first etching process of forming a first conductive layer pattern with a tapered sidewall portion of the laminate;

a plasma treatment to be performed to the first conductive layer pattern;

a second etching process of subjecting the first conductive layer pattern to anisotropic etching to form a second conductive layer pattern; and

a process of adding an impurity to the semiconductor layer with the second conductive layer and the third conductive layer in the second conductive layer pattern as a shielding mask to form a region to which the impurity is added in the semiconductor film, which overlaps with the first conductive layer in the second conductive layer pattern.

[Claim 24]

The method according to claim 23, wherein the plasma treatment is an argon plasma treatment.

[Claim 25]

The method according to claim 23, wherein a reaction product adhering to a sidewall portion of the first conductive layer pattern is removed by the plasma treatment.

[Claim 26]

The method according to claim 23, wherein the first conductive layer is metal nitride.

[Claim 27]

The method according to claim 23, wherein the third conductive layer is a metal having high-melting point.

[Claim 28]

A semiconductor device comprising a gate electrode comprising a lower first conductive layer and an upper second conductive layer including titanium or including titanium as its main component,

wherein a width of the first conductive layer is wider than that of the second conductive layer.

[Claim 29]

The semiconductor device according to clam 23, wherein the first conductive layer is metal nitride.

[Claim 30]

A semiconductor device comprising a gate electrode comprising a first conductive layer, a second conductive layer including titanium or including titanium as its main component on the first conductive layer, and a third conductive layer on the second conductive layer,

wherein a width of the first conductive layer is wider than those of the second conductive layer and the third conductive layer.

[Claim 31]

The semiconductor device according to clam 30, wherein the first conductive layer is metal nitride.

[Claim 32]

The semiconductor device according to clam 30, wherein the third conductive layer is a metal having high-melting point.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention belongs]

The present invention relates to a method of manufacturing an insulated gate field-effect transistor. In particular, the present invention relates to a method of manufacturing a semiconductor device, which can be applied to a thin film transistor (TFT) with a gate overlapping structure.

[0002]

[Prior Art]

In a display device using a liquid crystal, a product with a large-screen over 20 inches, which is typified by a liquid crystal display TV, has been put to practical use. In recent years, a liquid crystal display device integrated with a driving circuit has been realized with a TFT in which a polycrystalline silicon film is used as an active layer.

[0003]

However, a defect is pointed out that a TFT using a polycrystalline silicon film has a low withstanding pressure in drain junction to increase junction leak current (hereinafter, referred to as OFF-leak current). It is known that it is effective to form a lightly doped region (LDD) structure as measures for the defect.

[0004]

The phenomenon is pointed out as a problem that high electric field is generated in the vicinity of the drain region, then, a generated hot carrier is trapped by a gate insulating film on the LDD region, and then, device characteristics such as threshold voltage are greatly fluctuated and lowered. In order to prevent the deterioration due to hot carriers, a TFT in which a gate electrode is overlapped with an LDD region is disclosed (refer to Japanese Patent Laid-Open 2000-294787). The TFT with the gate overlapped LDD structure has higher current driving ability compared to a TFT with a normal LDD structure, and effectively eases the high electric field in the vicinity of the drain region to suppress the deterioration due to hot carriers.

[0005]

However, in the case of the TFT with the gate overlapped LDD structure

disclosed in the above publication, after an impurity region for forming an LDD region is formed in a semiconductor layer, a gate electrode is overlapped with the LDD region. Accordingly, the portion overlapping with the gate electrode cannot be accurately formed along with the miniaturization of design rule.

[0006]

As an appropriate example for manufacturing a TFT with a gate overlapping LDD structure in a self-aligning manner, the technique is disclosed that a conductive layer that has at least two layer laminated is subjected to exposure once and etching plural times to make the upper layer and the lower layer have different sizes, and then, ion doping is conducted with utilizing the differences in size and thickness to form an LDD region overlapped with a gate electrode in a self-aligning manner (for example, refer to Japanese Patent Laid-Open 2002-14337).

[0007]

Of course, it is necessary that a length of the LDD (a length with respect to the channel length) is optimized depending on driving voltage of the TFT in order to maximally show the function of the LDD overlapped with the gate electrode as measures against the deterioration due to hot carriers. Namely, there is an optimum length for easing effectively the high electric field in the vicinity of the drain region.

[0008]

[Problem to be solved by the Invention]

The technique disclosed in the above-mentioned publication has two steps: the first step of etching a conductive layer that has two layers laminated into a tapered shape and the second step of selectively subjecting only the upper layer of the conductive layer in the tapered shape to anisotropic etching, and is characterized in that a taper angle is controlled to enable controlling the length of the LDD.

[0009]

In order to drive a TFT with a channel length on the order of 10 μm at 10 to 20 V, the TFT needs to have an LDD with a length (a length of a portion overlapping with a gate electrode) at least 1 μm (preferably, at least 1.5 μm).

[0010]

In the conventional technique using a gate electrode that has a laminated structure of at least two layers, it is necessary that a taper angle (an angle with the substrate surface) of an edge be decreased in the stage of processing the gate electrode in order to control a length of an LDD. For that purpose, the mask pattern needs to be largely recessed.

[0011]

However, in the case of forming a gate electrode in which a first conductive layer of a two-layer laminated structure is tantalum nitride and the second conductive layer is titanium or metal including titanium as its main component, it is difficult to obtain a tapered shape that is necessary for getting the length of the LDD region at 1 μm or more, preferably, 1.5 μm by a taper etching process, that is, an increase of a taper angle of an edge of the conductive film becomes a problem. If an anisotropic etching process is conducted thereafter, a portion that is not etched (a skirt shape) is left at an edge of the second conductive layer to shorten a portion that functions as the LDD region. Also in the case of a three-layer laminated structure, a portion that is not etched (a skirt shape) is left as above to cause the same problem.

[0012]

For not only the gate electrode but also an edge portion or a sidewall portion of a film, it makes an etching process into a tapered-shape in accordance with a mask pattern possible that dry etching is used to etch the object to be processed while recessing a width of the mask pattern at the same time. For that purpose, the selection of a kind of gas for etching, the regulation of bias voltage, and the selective ratio of the film to a material of the mask pattern are important matters.

[0013]

Since the portion that is not etched is left at the edge of the second conductive layer in the anisotropic etching process after the taper etching process of the gate conductive layers of the two-layer or the three-layer laminated structure, with the result that the LDD region is shortened, it is an object of the present invention to reduce or remove the left portion that is not etched at the edge of the second conductive layer to get a necessary length as the LDD region.

[Means for solving the Problem]

[0014]

Since a sufficient taper cannot be obtained in a taper etching process, it is necessary to remove the left portion that is not etched at the edge of the second conductive layer (skirt shape) in order to make the LDD region longer as much as possible. According to the present invention, an argon plasma treatment is added between a taper etching process and an isotropic etching process to be performed to two-layer or three-layer laminated conductive layers to serve as reducing or removing a left portion that is not etched (skirt shape), which is generated at an edge of the second conductive layer by the isotropic etching process thereafter.

[0015]

The length of an LDD overlapping with a gate electrode (hereinafter, referred to as Lov for the sake of convenience), which is necessary for controlling degradation due to hot carriers, is considered as follows.

[0016]

First, the time until decrease of the maximum field-effect mobility by 10 % is defined as lifetime in the case where the Lov is a predetermined value to degradation of a TFT, and the voltage at which the lifetime becomes ten years is derived as ten-year guaranteed voltage from a linear relationship obtained by plotting the reciprocal of a drain voltage on a semilogarithmic graph, as shown in Fig. 10. For example, in Fig. 10, the ten-year guaranteed voltage of a TFT with a Lov of 1.0 μm is 16 V. A high-voltage power source often has 16V in a liquid crystal panel and it is required to obtain guaranteed voltage of 19.2 V or more, which has a margin of twenty percent. Fig. 9 is a graph in which thus obtained value of the estimated guaranteed voltage is plotted in the case where Lov has each of 0.5 μm, 0.78 μm, 1.0 μm, 1.5 μm, and 1.7 μm. Fig. 9 also shows a value of drain voltage as twenty-hour guaranteed voltage, at which the time until change in ON-state current of the TFT by 10 % is 20 hours in a bias stress test.

[0017]

Although degradation due to hot carrier effect is insignificant with low driving voltage, it becomes difficult to be negligible in the case of driving at 10 V or more. As is

clear from Fig. 9, it is necessary to make the Lov 1 μm or more, preferably, 1.5 μm or more in the case of the driving voltage of 16 V.

[0018]

In order to satisfy the above requirement, the present invention provides a method for manufacturing a semiconductor device, which forms an LDD overlapping with a gate electrode in a self-aligning manner, wherein a gate electrode is formed of a laminate that has a plurality of conductive layers, which is made into a shape in which a width of a lower first conductive layer is longer in the direction of a channel length than that of a second conductive layer, and the gate electrode is used as a mask during ion doping for forming the LDD. At this time, in order to make the LDD overlapping with the gate electrode 1 μm or more, and preferably, 1.5 μm or more, the present invention is characterized in that a shape of a mask pattern for forming the gate electrode is processed, and dry etching is combined to obtain an optimum shape.

[0019]

The present invention has a process of performing a first etching process for forming a first conductive layer pattern in which a sidewall portion of a laminate is tapered after a forming mask pattern on a laminate of metal nitride and one of titanium and metal including titanium as its main component, and a process of performing a second etching process for performing an isotropic etching to the first conductive layer pattern, wherein a plasma treatment with inert gas is performed between the first etching process and the second etching process.

[0020]

In the present invention, a laminated structure comprising a lower first conductive layer and an upper second conductive layer is formed over a semiconductor layer with a gate insulating film interposed therebetween, a mask pattern is formed on the laminated structure, argon plasma is irradiated after performing taper etching to the second conductive layer and the first conductive layer, and the second conductive layer in a first conductive layer pattern is selectively etched in accordance with the mask pattern to form a second conductive layer pattern in which a width of the first conductive layer in the direction of a channel length is different from that of the second conductive layer and

is longer. It becomes possible to make a projecting length of the first conductive layer 1 μm or more, which is used as a mask for shielding ions accelerated by an electric field to enable forming a lightly doped drain region overlapping with the first conductive layer pattern. In other words, the lightly doped drain region can be formed in a self-aligning manner. Of course, the second conductive layer pattern can be used as a gate electrode.

[0021]

In the invention as above, an appropriate combination of the first conductive layer and second conductive layer is that the first conductive layer is tantalum nitride and the second conductive layer is titanium or one of an alloy and a compound including titanium as its main component.

[0022]

In the present invention, a first conductive layer, a second conductive layer, and a third conductive layer are sequentially laminated over a semiconductor layer with a gate insulating film interposed therebetween to form a laminated structure, a mask pattern is formed thereon and a first conductive layer pattern that has tapered portions at respective edges is formed, argon plasma is irradiated after this taper etching process, and the third conductive layer and the second conductive layer in the first conductive layer pattern are selectively etched in accordance with the mask pattern to form a second conductive layer pattern in which a width of the first conductive layer in the direction of a channel length is different from that of the second conductive layer and is longer. It becomes possible to make a projecting length of the first conductive layer 1 μm or more, which is used as a mask for shielding ions accelerated by an electric field to enable forming a lightly doped drain region overlapping with the first conductive layer pattern. In other words, the lightly doped drain region can be formed in a self-aligning manner. Of course, the second conductive layer pattern can be used as a gate electrode.

[0023]

In the invention above, an appropriate combination of the first conductive layer, the second conductive layer, and third conductive layers is that the first conductive layer is tantalum nitride, the second conductive layer is titanium or one of an alloy and a compound including titanium as its main component, and the third conductive layer is

titanium nitride.

[0024]

[Embodiment Mode of the Invention]

Hereinafter, an embodiment mode of the present invention will be described in detail with reference to drawings. It should be understood that the invention is not limited to the following embodiment mode and that various modifications are permitted without departing from the spirit and scope thereof.

[0025]

[Embodiment Mode 1]

In the present mode embodiment, a process will be described, where a gate electrode is used as a mask during ion doping to form an LDD overlapping with the gate electrode in a self-aligning manner and make the length (Lov) 1 μm or more. More specifically, an argon plasma treatment is performed to a conductive layer of a taper sidewall portion of a tapered laminated structure after forming a first conductive layer pattern, and a second conductive layer pattern in a first conductive layer pattern is selectively etched in accordance with the mask pattern to form a second conductive layer pattern.

[0026]

In Fig. 1(A), a first insulating film (base film) 101, a semiconductor layer 102, and a second insulating film (gate insulating film) 103 are formed on a glass substrate 100, and a first conductive layer 104, a second conductive layer 105, and a third conductive layer 106 are formed thereon. A mask pattern 107 is formed with the use of a photoresist according to photolithographic processing.

[0027]

As the first conductive layer, a metal having high-melting point such as tantalum nitride (TaN) is formed to be a thickness from 30 to 50 nm, and the second conductive layer is formed of titanium or one of an alloy or a compound including titanium as its main component to be a thickness from 300 to 600 nm.

[0028]

For the third conductive layer, a metal having high-melting point such as

titanium nitride (TiN) is used. However, the third conductive layer is provided to lower contact resistance and is not the essential component required in the present invention. It makes processing easy to combine the second conductive layer of titanium or one of alloy or a compound including titanium as its main component since titanium nitride can be processed with the same etching gas as that for titanium.

[0029]

Next, as shown in Fig. 1(B), the second conductive layer 105 and the third conductive layer 106 are etched dry etching. As etching gas, gas of CF_4, Cl_2, and O_2 is used. To increase an etching rate, a dry etching system that uses a high-density plasma source such as ECR (Electron Cyclotron Resonance) or ICP (Inductively Coupled Plasma) is used.

[0030]

The mask pattern 107 formed of resist is sputtered by ions accelerated by an electric field, and a reaction by-product adheres to the sidewall of the workpiece. This is also called a sidewall protective film, and the reason why the second conductive layer including titanium as its main component is tapered in the process at this stage is to remove the sidewall protective film. Namely, since the reaction by-product is hardly deposited on the sidewall when anisotropic etching is thereafter performed to a tapered second conductive layer 105 as shown in Fig. 3(A), it is possible to perform the etching process without leaving residue to form patterns of the second and third conductive layers 105' and 106' as shown in Fig. 3(B). On the other hand, when the sidewall of the second conductive layer 105 is substantially vertical as shown in Fig. 4(A), a reaction by-product is deposited during the etching process, and the reaction by-product remains when an anisotropic etching is performed thereafter, as shown in Fig. 4(B). In other words, when at least the second conductive layer is tapered at this stage, the sidewall protective film can be removed.

[0031]

Next, the etching gas is changed to CF_4 and Cl_2 to etch tantalum nitride that is the first conductive layer. Of course, all of the conductive layers may be etched at the same time. However, it is necessary to set longer etching time in consideration of

fluctuation in etching rate in etching the second conductive layers 105 with the thick film thickness. In that case, a base is etched to become extremely thin when the base is silicon oxide. In order to prevent this, two steps of etching processes are performed in this way.

[0032]

In this way, a first conductive layer pattern 108 comprising first conductive layer 104', second conductive layer 105', and third conductive layer 106' is formed on the second insulating film 103, as shown in Fig. 1(C). The angle made by the tapered shape at the edge and a surface of the substrate 100 is made 10 to 20 degrees. Although the angle is determined depending mainly on the relations with the film thickness of the second conductive layer, the length occupied by the tapered portion is made about 0.5 to 1.5 μm.

[0033]

After the taper process of the respective conductive films, an argon plasma treatment is performed to remove a reaction product adhering to the taper sidewall. When this argon plasma treatment is not performed, the reaction product becomes a stopper later in trying a process under anisotropic etching conditions to leave a portion that is not etched (skirt shape) at an edge of the second conductive layer, and it is hard to form an intended shape, which is near to perpendicularity as mush as possible. The argon plasma treatment after the taper process is necessary for preventing the portion that is not etched from being left at the edge of the second conductive layer. (Fig. 1(D))

[0034]

Then, with the use of BCl_3, Cl_2, and O_2 as etching gas, the second conductive layer 105' and the third conductive layer 106' are selectively etched in accordance with a mask pattern 107'. In this case, the bias voltage to be applied to the substrate side is lowered to thereby leave the first conductive layer 104'. The edge of the second conductive layer 105' is recessed inward from that of the first conductive layer 104', and the length of Lov is determined depending on the recess amount, as will be described later. In this manner, a second conductive layer pattern 109 comprising the first conductive layer 104', a second conductive layer 105", and the third conductive layer 106" are formed, which becomes a gate electrode at a portion intersecting with the semiconductor

layer 102 (Fig. 1(E)).

[0035]

The addition of an impurity with one conductivity type to the semiconductor film 103, that is, the formation of an LDD and a source/drain region can be performed in a self-aligning manner with the use of the second conductive layer pattern 109. Fig. 2(A) shows a doping process for forming an LDD that overlaps with the gate electrode, wherein an ion of the impurity with the one conductivity type is made to pass through the first conductive layer 104' and added to the semiconductor layer 102 positioned in the lower layer portion to form an one conductivity type impurity region 110 with a first concentration. In this case, an acceleration voltage of 50 kV or more is required depending on the film thicknesses of the second insulating film and the first conductive layer. The concentration of the impurity in the one conductivity type impurity region 110 with the first concentration is set from 1×10^{16} to $5 \times 10^{18}/cm^3$ (peak value) on the premise of the LDD.

[0036]

In the doping process for forming the source/drain region, the second conductive layer pattern 109 is used as a mask for shielding ions and an one conductivity type impurity region 111 with a second concentration is formed outside the one conductivity type impurity region 110 with the first concentration. In this case, the acceleration voltage is set at 30 kV or less. The concentration of the impurity in the one conductivity type impurity region 111 with the second concentration is set at 1×10^{19} to $5 \times 10^{21}/cm^3$ (peak value). (Fig. 2(B))

[0037]

After that, a third insulating film 112 using silicon nitride, a fourth insulating film 113 using an organic compound material of low-dielectric constant, and a wiring 114 are formed. (Fig. 1(C))

[0038]

As described above, according to the present embodiment mode, it is possible to form an LDD overlapping with a gate electrode in a self-aligning manner and to form a TFT with the length (Lov) of 1 μm or more with the use of the gate electrode as a mask

during ion doping. The length of the LDD region overlapping with the gate electrode is 1 μm or more to make a structure that is hard to degrade due to hot carriers.

[0039]

[Embodiments]

(Embodiment 1)

In the present embodiment, an example of forming a gate electrode according to a process based on the embodiment mode will be described. The present embodiment will be described with reference to Fig. 1.

[0040]

First, the first insulating layer 101 is formed of a silicon oxynitride film of 150 nm in thickness on the aluminosilicate-glass substrate with plasma CVD. The semiconductor layer 102 is formed of a crystalline silicon film for which an amorphous silicon film of 50 nm in thickness is crystallized by laser annealing so as to be isolated and separated into the shape of an island. As the second insulating film 103, a silicon oxynitride film of 115 nm in thickness is formed by plasma CVD with the use of SiH_4 and N_2O as source gas. The first conductive layer 104 formed of tantalum nitride is made 30 nm in thickness, the second conductive layer 105 formed of titanium is made 320 nm in thickness, and the third conductive layer 106 formed of titanium nitride is formed to be a thickness of 50 nm. The mask pattern 107 is formed of a positive photoresist to be a thickness of 1.5 μm. Although the width of the mask pattern may be set appropriately, photolithographic processing is performed with mask patterns with 4.5 μm and 10 μm in the present embodiment (Fig. 1(A)).

[0041]

Next, the second conductive layer (titanium) 105 and the third conductive layer (titanium nitride) 106 are etched by dry etching. For etching, an ICP etching system is used. Fig. 5 shows the configuration of the ICP etching system. A reaction chamber 801 is connected to a gas supply means 803 for etching and an exhaust means 804 for maintaining reduced pressure in the reaction chamber 801. A plasma generation means comprising a spiral coil 802 for inductively coupling to the reaction chamber 801 through a quartz plate and a high-frequency (13.56 MHz) power supply means 805. The

application of bias voltage to the substrate side is conducted by a high-frequency (13.56 MHz) power supply means 806 to generate self-bias to a stage with the substrate thereon. For the etching process, the kind of etching gas to be supplied, high-frequency power supplied from each of the high-frequency (13.56 MHz) power supply means 806 and 807, and etching pressure are main parameters.

[0042]

For the etching process in Fig. 1(B), gas of CF_4, Cl_2, and O_2 is used as etching gas. The etching pressure is set at 1.3 Pa, and each of 500 W of power for generating plasma and 300 W of power for biasing the substrate is supplied. Subsequently, as shown in Fig. 1(C), the etching gas is changed to CF_4 and Cl_2 to etch tantalum nitride that is the first conductive layer. The etching condition in this case, each of 1.5 Pa of etching pressure, 500 W of power for generating plasma, and 10 W of power for biasing the substrate is supplied. In this way, the first conductive layer pattern 108 can be formed.

[0043]

After that, an argon plasma treatment is performed to remove or reduce a reaction product (TiOx) adhering to a taper sidewall portion of the first conductive layer pattern 108, which is considered a stopper film. In the argon plasma treatment, the ICP etching system is used as well, argon is supplied at 150 sccm, and each of 450 W of power for generating plasma and 100 W of power for biasing the substrate is supplied under a pressure of 2.0 Pa to perform the treatment for 30 sec.

[0044]

Next, anisotropic etching is performed with the use of BCl_3, Cl_2, and O_2 as etching gas to process mainly the second conductive layer 105'. The etching pressure is set at 1.9 Pa, and each of 500W of power for generating plasma and 10 W of power for biasing the substrate is supplied. The edge of the second conductive layer 105' is recessed inward from the edge of the first conductive layer 104'. In this way, the second conductive layer pattern 109 is formed, which becomes a gate electrode at a portion intersecting with the semiconductor layer 102. The recess width from the edge of the first conductive layer 104' can be made 1 μm or more. As shown in Fig. 6, the recess width d becomes a length that determines the length of Lov.

[0045]

Figs. 7 and 8 are images through scanning electron microscopy (SEM), showing typical processed shapes in the case of performing an argon plasma treatment and an anisotropic etching process after a taper process, which each shows a state in which a tantalum nitride layer, a titanium layer, a titanium nitride layer, and resist that is a mask material are laminated from the bottom layer. Although the diagrams show the SEM images observed at an angle and from a section, a recess width of the titanium layer or a projecting width of the titanium nitride layer is estimated to be about 1.0 μm.

[0046]

Thereafter, the one conductivity type impurity region 110 with the first concentration for forming the LDD is doped with phosphorous or boron at a concentration from 1×10^{16} to $5 \times 10^{18}/cm^3$ (peak value) under an acceleration voltage of 50 kV by ion doping. (Fig. 2(A))

[0047]

Besides, in the doping process for forming a source/drain region, the second conductive layer pattern 109 is used as a mask for shielding ions and the one conductivity type impurity region 111 with the second concentration is formed outside the one conductivity type impurity region 110 with the first concentration, in this case, at the acceleration voltage of 10 kV and the concentration of phosphorous or boron at 1×10^{19} to $5 \times 10^{21}/cm^3$ (peak value). (Fig. 2(B))

[0048]

After that, silicon oxynitride containing hydrogen is formed with plasma CVD to be a thickness of 100 nm, and photosensitive or non-photosensitive acrylic or polyimide resin is formed to be a thickness of 1 μm, thereby forming the fourth insulating film 113. Furthermore, the wiring 114 is formed according to need.

[0049]

In this way, the LDD overlapping with the gate electrode can be formed in a self-aligning manner, and also, the TFT with the length (Lov) of 1 μm or more can be formed.

[0050]

(Embodiment 2)

The present invention can apply to semiconductor devices in which various display screens are provided, and is useful particularly for large-screen semiconductor devices that have display screens more than 20 inches diagonally.

[0051]

Fig. 12 is a structural example of a semiconductor device that has a display panel 901 mounted in a casing 900, which is applicable to television receivers and monitor systems of computers. In the casing 900, an electronic circuit board 902 and a speaker 903 for sound reproduction are loaded, wherein the electronic circuit board 902 incorporates an amplifier and a high-frequency circuit formed of a semiconductor integrated circuit, and a semiconductor memory or a magnetic memory such as a hard disk as a memory function to fulfill a function of displaying an image.

[0052]

A display panel 901 can be composed of a driver-integrated type in which an active matrix pixel circuit 904 in which gate overlapping TFTs according to the present invention are used to arrange the TFT in a matrix shape, a scanning line driving circuit 905, and a data line driving circuit 906 are formed integrally.

[0053]

Fig. 11 is a diagram showing a principal structure of the active matrix pixel circuit 904. A gate electrode 302 intersecting with a semiconductor layer 301 and a data signal line 303 are formed of the same layer, that is, which is formed of a laminate including at least a conductive layer including titanium as its main component, and an etching process for forming the gate electrode or the wiring pattern is performed according to Embodiment 1. In this manner, it is possible to form a gate overlapping TFT that has Lov with a length of 1 μm or more, and also, resistance of the data signal line can be lowered. A gate signal line 304 is formed in the above thereof with an interlayer insulating film interposed therebetween and has a structure in contact with the gate electrode 302 through a contact hole. Of course, this wiring can be formed of titanium and aluminum, and it is possible to realize lowering resistance of the wiring. It is also possible to form a wiring 305 that connects the data signal line 303 and the semiconductor layer 301 of the same layer as the gate signal line 304. A pixel electrode 306 is formed

with the use of ITO (indium tin oxide) that is a compound of indium oxide and titanium oxide. The details of such pixels are disclosed in Japanese Patent Laid-Open 2001-313397.

[0054]

In the present embodiment, an example has been shown in the semiconductor device. However, the invention is not limited to the present embodiment and can be applied to various semiconductor devices. It is possible to be applied to various fields, for example, in addition to navigation systems, sound reproducing systems (such as car audio systems and component audio systems), notebook-sized personal computers, game machines, personal digital assistants (such as mobile computers, cellular phones, portable game machines, and electronic books), electrical home appliances such as refrigerators, washing machines, rice cookers, fixed telephones, vacuum cleaners, and clinical thermometers, railroad wall banners, and information displays such as arrival and departure guide plates in railroad stations and airports.

[0055]

Although the embodiments according to the invention have been described as above, it is to be understood by those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the present invention.

[0056]

[Effect of the Invention]

As described above, according to the present invention, in the process of forming a gate electrode of a laminate comprising a plurality of conductive layers to have a shape in which a width of a first conductive layer in the direction of a channel length is longer than that of a second conductive layer, the defect of a portion that is not etched (skirt shape) due to causing etch stop on the way is prevented from being left at an edge of the second conductive layer in an isotropic etching process by providing an argon plasma treatment for reducing or removing a reaction product after a taper etching process. As the result of no left portion that is not etched (skirt shape) at the edge of the second conductive layer, it is possible to make the length of the first conductive layer 1 μm or

more in the direction of the channel length. The use of the gate electrode as a mask during ion doping allows the length of an LDD region overlapping with the gate electrode to be 1 μm or more and to increase the lifetime against degradation due to hot carriers.

[0057]

According to the present invention, it is possible to form an LDD overlapping with a gate electrode in a self-aligning manner and to form a TFT with the length (Lov) of 1 μm or more with the use of the gate electrode as a mask during ion doping. The length of the LDD region overlapping with the gate electrode is 1 μm or more to enable increasing the lifetime of the TFT against degradation due to hot carriers.

[Brief Description of the Drawings]

[Fig. 1] sectional views for describing a process for making a semiconductor device according to the present invention

[Fig. 2] sectional views for describing a process for making the semiconductor device according to the present invention

[Fig. 3] diagrams for describing an effect of removing a reaction by-product by taper etching

[Fig. 4] diagrams for describing an effect of a reaction by-product in the case where the taper etching is not performed

[Fig. 5] a diagram for describing a configuration of an ICP etching device

[Fig. 6] a diagram for describing the relation between a recess width d of a second conductive layer and a length of Lov of a gate overlapping TFT

[Fig. 7] an SEM image in viewing at an angle a shape of a conductive layer pattern subjected to an etching process in accordance with Embodiment 1

[Fig. 8] an SEM image showing a sectional shape of a conductive layer pattern subjected to an etching process in accordance with Embodiment 1

[Fig. 9] a graph showing a dependency of an estimated guaranteed voltage (10 % deterioration of ON-state current) on a length of Lov

[Fig. 10] a characteristic diagram for estimating a lifetime of a TFT in accordance with a bias stress test and a graph showing a dependency on Lov

[Fig. 11] a top view showing active-matrix type pixels of a semiconductor device

according to the present invention

[Fig. 12] a diagram showing an example of a semiconductor device